control unit 3 reads the error-corrected data from the error corrector 61 and writes them to the buffer memory 4.

Step (f-19): the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 in order to check to see that the error-corrected data contain no error, and provides instructions for data transfer from the buffer memory 4 to the error detector 72. This data transfer involves data from the code word indicated by the error-containing code word signal 23 outputted together with the error-containing code detection signal 22 outputted first by the syndrome calculator 5 at step (f-4).

Step (f-20): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the error detector 72.

Step (f-21): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector 72 so as to supply the data read from the buffer memory 4.

Step (f-22): using the mid-term results of the error detection stored in the third mid-term register 83, the error detector 72 executes error detection of the transferred subsequent data, and transmits the error detection signal 21 to the system control unit 1 so as to inform whether an error has been detected or not.

The error correction for one sector is completed by repeating steps (f-13) through (f-22) 13 times, and the horizontal error correction for one ECC block is completed by repeating this procedure for 16 sectors. In the

third-time error correction, if the mid-term results of error detection obtained in the first-time error correction and stored in the third mid-term register 83 are valid, the number of repetition can be lessened in accordance with the position of the code word from which the error-containing code has been detected in the first-time error correction. This is the advantage of the present embodiment.

For example, in the second-time error correction shown in Figure 17, when error-containing codes are all contained in or after the sixth line of the second sector, the mid-term results of the EDCs held in the mid-term result register 81 are valid. With the use of the mid-term results, data transfer is started from the sixth code word in the second sector so as to perform syndrome calculation and error detection.

However, when an error-containing code is contained before the fifth line of the second sector, namely, in the second line of the second sector, the mid-term results of the EDCs become invalid. In this case, data transfer is started from the head of the second sector that is the sector following the sector (the first sector in this case) in which there is no error to be corrected in the second-time error correction.

Since the EDC calculation is performed one sector at a time, the start of data transfer is restricted to the head of a sector, using the error-containing code word signal and the error correcting position signal as data indicating the sector having an error-containing code. This can reduce the number of registers to hold the first-time mid-term results although more amount of data must be transferred for correction again than in the case where the start of the data transfer is indicated in code

word units.

Finally, steps (f-19) through (f-22) are executed once so as to terminate the error detection of one ECC block. In this case, the data transfer from the buffer memory 14 to the error detector 7 is started from the code word indicated by the error-containing code word signal 23 first outputted from the syndrome calculator 5 in the third-time error correction.

This effect shown in Embodiments 1 through 3 is also provided by the present embodiment.

As described hereinbefore, in the present embodiment, three-time error correction with the single error corrector 6 is performed by transferring data to the error detector 7 at the same time as the data transfer from the buffer memory 4 to the syndrome calculator 5. Until an error-containing code is detected by the syndrome calculator 5, error detection is executed in parallel with the syndrome calculation. In the error detection after the error corrector 6 has corrected an error, the mid-term results of error detection obtained before the detection of the error-containing code are used. This eliminates the need for all data in one ECC block being transferred from the buffer memory 4 to the error detector 7, thereby enabling an error detecting process to be started from a halfway point. This greatly reduces the time required for error correction and the power consumption in the same manner as in the present embodiment.

Although the present embodiment describes three-time error correction, it can be more than three times. It goes without saying that